What is claimed is:

1. A method for generating a fully depleted body structure in a silicon-on-insulator device having a substrate, the method comprising:
providing an extractor contact coupled to the body structure; and
providing an extractor voltage such that the extractor contact is reverse biased and minority carriers in the body structure are removed.

2. The method of claim 1 wherein the substrate is at ground potential.

3. The method of claim 1 wherein the extractor contact is coupled to a p-type silicon on the insulator.

4. The method of claim 1 wherein the extractor contact is coupled to an n-type silicon on the insulator.

5. The method of claim 1 wherein the silicon-on-insulator device has a drain region and the method further comprises applying a drain voltage to the drain region.

6. The method of claim 5 wherein the extractor voltage is greater than the drain voltage.

7. The method of claim 2 wherein the extractor voltage is less than the substrate potential.

8. A method for generating a fully depleted body structure in a PMOS silicon-on-insulator device having a substrate, a control gate, a drain region, and a source region, the method comprising:
applying an extractor voltage to an extractor contact coupled to the body structure; and

applying a substrate voltage to the substrate such that the extractor voltage is greater than the substrate voltage.

9. The method of claim 8 wherein the substrate voltage is ground potential.

10. The method of claim 8 wherein the extractor contact is coupled to an n-type silicon on the substrate.

11. The method of claim 8 and further including applying a positive voltage to the control gate to erase a charge stored in the device.

12. A method for generating a fully depleted body structure in an NMOS silicon-on-insulator device having a substrate, a control gate, a drain region, and a source region, the method comprising:
applying an extractor voltage to an extractor contact coupled to the body structure; and
applying a substrate voltage to the substrate such that the extractor voltage is less than the substrate voltage.

13. The method of claim 12 wherein the extractor contact is coupled to a p-type silicon on the substrate.

14. The method of claim 12 and further including applying a negative voltage to the control gate to erase a charge stored in the device.

15. A method for generating a fully depleted body region in an NROM flash memory device using a silicon-on-insulator structure, the device having a substrate, a control gate, a drain region, and a source region, the method comprising:
applying an extractor voltage to an extractor contact coupled to the body structure; and

applying a substrate voltage to the substrate such that the extractor voltage is less than the substrate voltage.

16. The method of claim 15 wherein the extractor contact is comprised of a p-type silicon.

17. A transistor having a silicon-on-insulator structure on a substrate, the transistor comprising:

a drain region comprising a first doped material and formed in the silicon-on-insulator;

a source region comprising the first doped material and formed in the silicon-on-insulator;

a control gate formed above and substantially between the drain and source regions; and

an extractor contact comprising a second doped material and coupled to a depletion region substantially between the drain and source regions, the depletion region being fully depleted in response to a reverse bias of the extractor contact.

18. The transistor of claim 17 wherein the first doped material is comprised of n-type silicon and the second doped material is comprised of p-type silicon.

19. The transistor of claim 17 wherein the first doped material is comprised of p-type silicon and the second doped material is comprised of n-type silicon.

20. A vertical multiple bit memory cell having a silicon-on-insulator structure on a substrate, the memory cell comprising:

a vertical metal oxide semiconductor field effect transistor (MOSFET) extending horizontally outward from a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain

regions, and a gate separated from the channel region by a high dielectric constant gate insulator that can store a first charge in a first storage region and a second charge in a second storage region;

a first transmission line coupled to the first source/drain region;

a second transmission line coupled to the second source/drain region; and

an extractor contact coupled to the channel region such that a reverse bias on the extractor contact fully depletes the channel region.

21. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes a memory array having a plurality of memory cells with a silicon-on-insulator structure, each memory cell comprising:

a drain region comprising a first doped material and formed in the silicon-on-insulator;

a source region comprising the first doped material and formed in the silicon-on-insulator;

a control gate formed above and substantially between the drain and source regions; and

an extractor contact comprising a second doped material and coupled to a depletion region substantially between the drain and source regions, the depletion region being fully depleted in response to a reverse bias of the extractor contact.

22. The electronic system of claim 21 wherein the memory cell is a vertical memory cell.